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Intel(R) Firmware Support Package (Intel(R) FSP) for Intel (R) Bay Trail Release Notes

MR5 Release - Release Notes
Dec 21 2015

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RELEASE NOTES CONTENTS

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1. OVERVIEW
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This package contains the binary image(s) and collaterals for the Intel(R) Firmware Support Package (Intel(R) FSP) for Intel (R) Bay Trail.

This FSP binary has been integrated and validated with a Reference Boot Loader on a Bayley Bay CRB with Bay Trail SOC.

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2. RELEASE INFORMATION
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This release supports the Intel(R) Bay Trail SOC and is compliant with FSP 1.0
External Architecture Specification. This release package contains

- FSP Binary
- Boot Setting File (BSF)
- Integration Guide
- Release Notes

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3. INTEGRATION NOTES
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This release of the FSP has been validated with a reference bootloader on a
Bayley Bay Customer Reference Platform.

The reference bootloader with this FSP integrated can be downloaded from CDI/IBL.
However the FSP can also be integrated with any other bootloader of choice and
the integration requirements are documented in the Atom E3800 FSP Integration Guide
- 519985_Atom_E3800_FSP_Integr_Guide-rev1-9.pdf

When secure boot feature is enabled, integration of the FSP requires additional
steps in addition to the steps documented in the integration guide. Please refer
to Secure Boot Readme - README.coreboot_secureboot.txt. And for more detailed
information please refer to
#558081_Enabling_Secure_Boot_with_Intel_FSP_and_

coreboot_for_Intel_Atom_Processor_E3800_Product_Family_Implementation_Guide-
Rev-1.0.pdf

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4. SOC FEATURES
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- Upto 4 CPU Cores
- Upto 2.2 GHz CPU Frequency
- HDMI, DP/eDP, VGA Display
- 8 GB Max Addressable Memory @ 1066/1333 MT/s
- If only 1 DIMM is used, channel 0 must be used.
- Both memory channels must be populated with DIMMs of same configuration.
- PCI Express
- SATA
- USB 3.0
- Serial Peripheral Bus Controllers

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5. SUPPORTED FEATURES
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- Bay Trail-I SOC B2/B3/C0/D0 steppings
- MCU update
- Memory Detection and Initialization
- Fast Boot support
- MTRR Initialization on all CPU threads
- PCI Express initialization
- SOC Internal devices initialization
- Configuration Options through Intel BCT
- Rebase to a different base address through Intel BCT
- Secure Boot
- S3 resume
- PCI mode and ACPI Mode for the LPSS devices
- USB 3.0 support

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6. FSP Configuration
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When integrating with a bootloader the FSP should be placed at the same base
address that it is configured to.

The default base address for this FSP is 0xFFFC0000. The base address for the
FSP can be configured to a different address using the Intel BCT.

The FSP also provides a set of configuration options for initializing the SOC
and can be customized through the Intel BCT.

The latest Intel BCT can be found from the website www.intel.com/fsp.

Note: For BCT version 3.1.3, it needs run as administrator.

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7. LIMITATIONS

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None.

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8. KNOWN ISSUES

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None.

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9. CHANGE LOG

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Maintenance Release 6
-None

Maintenance Release 5
- Added ASR support
- Added SEC Unconfig Status check
- Upgraded IntelFspPkg to the latest
- Fixed the system hang in POST code 0x0C when DELAY_PCIE_RLS is enabled
- Disable PCIe root ports which have been configured as disabled in soft-strap
- Updated MpInit driver for APs wakeup slowly condition. Waiting time can be
  configured by UPD options APTaskTimeoutCnt

Gold 004 Release
- Added new option to disable/enable the integrated graphics
- Synced up to the latest BIOS silicon reference code

Gold 003 Release
- C0/D0 Stepping support
- MRC version 1.0
- Added option for IgdRenderStandby
- Moved Memory down parameters to UPD section
- Added Android Support

Gold 002 Release
 - Minor Update

Gold 001 Release
- B3 stepping support
- Bakersport platform support (ECC platform)

Beta 002 Release
- USB 3.0 support
- Fixed S3 issue

Beta 001 Release
- Bay Trail B0 support
- Secure Boot support